GF40: 5V Oscillators

Libraries

Name	Process	Form Factor
RGO_GF40_25V5_LP_20C_OSC	LP	Staggered CUP
RGO_GF40_25V5_LP_40C_OSC	LP	Inline CUP

Summary

The 5V Oscillators library provides oscillator I/O cells designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal.

- 32 kHz Real Time Clock Oscillator
- 100 MHz programmable wide-range oscillator

This 40nm library is available in both staggered CUP and inline CUP wire bond implementations with a staggered flip chip option.

To design an operational I/O power domain with these cells, an additional library is required – 3.3V Wide-Range GPIO. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a functional pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 200V ESD Machine Model (MM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

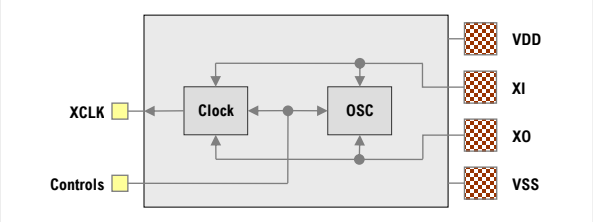
- Staggered (pad-limited) – 120µm x 200µm
- Inline (core-limited) – 200µm x 135µm

Recommended operating conditions

Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.90	1.0	1.10	V
		0.99	1.1	1.21	V
		1.08	1.2	1.26	V
V_{DVDD}	I/O supply voltage	4.5	5.0	5.5	V
T_J	Junction temperature	-40	25	175	°C
V_{PAD}	Voltage at PAD	0	-	V_{VDD}	V

[1] XI can be driven by an external clock.
XO should never be driven or loaded by anything other than the oscillator crystal.

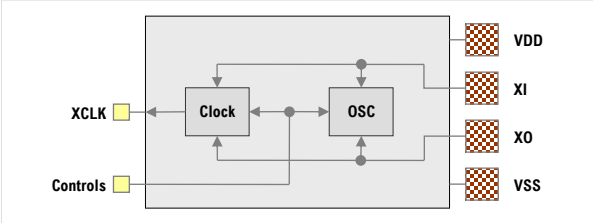
OSx_BI_032_1250V



32kHz RTC Oscillator Features

- Designed to use a 32.768 kHz external crystal
- Optimized for stability and minimum jitter
- Low power (4µW typ)
- Characterized with 8pF to 44pF crystal loading capacitors at each port (XI / XO)
- Speed-up circuitry for fast startup
- Power-down mode
- Bypass mode
- Operates on core power only (VDD / VSS cells embedded)

OSx_BI_100_1250V



100 MHz Programmable Oscillator Features

- Programmable drive strength – wide frequency range
- Low self-noise – optimized for stability and minimum jitter
- Frequency range – ≥ 1 MHz to 100 MHz
- Characterized with industry-standard crystals
- Power-down mode
- Forced bypass mode
- Low power - operates on core power only
- VDD / VSS cells embedded

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 5V	Temperature
1.2	FF	+5%	+10%	-40°C
	FFF	+5%	+10%	125°C
	FFF	+5%	+10%	150°C
	FFF	+5%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C
1.1 / 1.0	FF	+10%	+10%	-40°C
	FFF	+10%	+10%	125°C
	FFF	+10%	+10%	150°C
	FFF	+10%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C

Published by:

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